Patent Claims

1. A method for operating semiconductor chips, particularly memory chips, which are arranged in groups on modules (M1-M4) which are connected to a common data bus (DQ),
where each semiconductor chip (IC1-IC36) on each module (M1-M4) is connected to at least one data line (DQ1-DQ72) in the data bus (DQ),
having the following method steps:
a) a group of semiconductor chips (IC1-IC36) is selected from semiconductor chips (IC1-IC36) arranged on the modules (M1-M4) on the basis of a prescribed selection criterion independently of module, the selected group of semiconductor chips (IC1-IC36) using the data lines (DQ1-DQ72) in the data bus (DQ) over the entire bus width;
b) the semiconductor chips (IC1-IC36) in the selected group are activated; and
c) data interchange is performed between the data lines (DQ1-DQ72) in the data bus (DQ) and the selected group of semiconductor chips (IC1-IC36).

2. The method as claimed in claim 1,
where method steps a) to c) are repeated and different semiconductor chips (IC1-IC36) are selected in method step a) in the course of two cycles taking place at successive times.

3. The method as claimed in claim 1 or 2,
where the selection criterion is the temperature of the semiconductor chips (IC1-IC36), and preferably semiconductor chips (IC1-IC36) having the lowest temperature are selected.

4. The method as claimed in one of claims 1 to 3,
where the semiconductor chips (IC1-IC36) are selected using a statistical method.

5. The method as claimed in claim 4, where the statistical method takes into account the arrangement of the semiconductor chips (IC1-IC36) on the modules (M1-M4) and/or the arrangement of the modules (M1-M4) in relation to one another or in relation to other adjacent components.

6. The method as claimed in claim 4 or 5, where the statistical method takes into account empirically obtained and/or currently ascertained data.

7. The method as claimed in one of claims 1 to 6, where each of the semiconductor chips (IC1-IC36) has an associated selection probability.

8. The method as claimed in claim 7, where the semiconductor chips (IC1-IC36) are arranged in three dimensions with respect to one another, where the selection probability for a semiconductor chip (IC1-IC36) depends on its relative situation with respect to adjacent semiconductor chips (IC1-IC36), and a semiconductor chip (IC1-IC36) in an outer region of the modules (M1-M4) has a higher selection probability than a semiconductor chip (IC1-IC36) in an inner region.

9. The method as claimed in one of the preceding claims, where each of the semiconductor chips (IC1-IC36) arranged on the modules (M1-M4) has an associated individual index (CRS) which denotes the corresponding module (M1-M4) and the position of the corresponding semiconductor chip (IC1-IC36) on the module (M1-M4), where the indices (CRS) for the group of semiconductor chips (IC1-IC36) which was selected independently of module in method step a) are stored in a register device (RL),

where the indices (CRS) for the semiconductor chips (IC1-IC36) associated with the corresponding group are read from the register device (RL) in method step b) and the corresponding semiconductor chips (IC1-IC36) are activated using their indices (CRS).

10. The method as claimed in one of the preceding claims,
where method steps a) to c) take place at the beginning of a startup procedure in which the semiconductor chips (IC1-IC36) are started up.

11. The method as claimed in one of the preceding claims,
where the semiconductor chips (IC1-IC36) are memory chips, and
where method steps a) to c) take place at a time at which the content of the memory chips (IC1-IC36) is redundant.

12. The method as claimed in one of the preceding claims,
where the semiconductor chips (IC1-IC36) are memory chips, and
where the data already stored in the memory chips (IC1-IC36) are stored in a buffer store (HD) before a group of memory chips (IC1-IC36) is selected in method step a).

13. The method as claimed in one of the preceding claims,
where, besides the group of semiconductor chips (IC1-IC36) which is selected in method step a), a further group of further semiconductor chips (IC1-IC36) is selected independently of module, and the semiconductor chips (IC1-IC36) in this further group likewise use the data lines (DQ1-DQ72) in the data bus (DQ) over the entire bus width, and

where the data interchange between the data lines (DQ1-DQ72) in the data bus (DQ) and the semiconductor chips (IC1-IC36) in a group in method step c) involves alternating between the groups of semiconductor chips (IC1-IC36).

14. A control apparatus for semiconductor chips, particularly memory chips, which are arranged in groups on modules (M1-M4) which are connected to a common data bus (DQ),
where each semiconductor chip (IC1-IC36) on each module (M1-M4) is connected to at least one data line (DQ1-DQ72) in the data bus (DQ),
where a selection device (E) is designed in order to select the semiconductor chips (IC1-IC36) for the group cyclically on the basis of a prescribed selection criterion independently of module, and
where an activation device (A) is designed in order to activate the semiconductor chips (IC1-IC36) in the selected group for data interchange with the data lines (DQ1-DQ72) in the data bus (DQ).

15. The control apparatus as claimed in claim 14,
where the selection device (E) is designed in order to select the semiconductor chips (IC1-IC36) for the active group on the basis of the temperature of the semiconductor chips (IC1-IC36).

16. The control apparatus as claimed in claim 14 or 15,
where the selection device (E) is designed in order to select the semiconductor chips (IC1-IC36) for the active group using a statistical method.

17. The control apparatus as claimed in one of claims 14 to 16,
where the selection device (E) is designed in order to assign each semiconductor chip (IC1-IC36) an individual

selection probability on the basis of its relative situation in a three-dimensional arrangement of the semiconductor chips (IC1-IC36).

18. The control apparatus as claimed in one of claims 14 to 17,
where an assessment device (S) is designed in order to assess the semiconductor chips (IC1-IC36) according to prescribed criteria, particularly the temperature, and
where the selection device (E) is designed in order to select the semiconductor chips (IC1-IC36) on the basis of the assessment results from the assessment device (S).

19. The control apparatus as claimed in one of the preceding claims,
where the activation device (A) is designed in order to activate the semiconductor chips (IC1-IC36) in the active group using an index (CRS) which is individually associated with each semiconductor chip (IC1-IC36) and denotes the corresponding module (M1-M4) and the position of the corresponding semiconductor chip (IC1-IC36).

20. The control apparatus as claimed in one of the preceding claims,
where a register device (RL) is designed in order to store the information about the association between the semiconductor chips (IC1-IC36) and the active group of semiconductor chips (IC1-IC36).

21. An arrangement for operating memory chips (IC1-IC36) which are arranged in groups on modules (M1-M4) which are connected to a common data bus (DQ),
where each memory chip (IC1-IC36) on each module (M1-M4) is connected to at least one data line (DQ1-DQ72) in the data bus (DQ),

having a control apparatus (C) for controlling data interchange between the data lines (DQ1-DQ72) in the data bus (DQ) and the memory chips (IC1-IC36), comprising a selection device (E) for the purpose of selecting a group of memory chips (IC1-IC36) for data interchange with the data bus (DQ) on the basis of a prescribed selection criterion independently of module, and an activation device (A) for the purpose of activating the memory chips (IC1-IC36) in the selected group for data interchange with the data lines (DQ1-DQ72) in the data bus (DQ),

having a buffer store (HD) for the purpose of buffer-storing the data already stored in the memory chips (IC1-IC36) while the group of memory chips (IC1-IC36) is being reorganized.